Ronald Selman

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OBJECTIVE: Electrical Engineering

SUMMARY: Over 12.5 years experience designing world class electronics. Has rigorous technical expertise in digital, analog, and programming disciplines with many significant contributions to new product releases, from inception of design concept through pilot manufacturing runs. High volume productivity in assignments and maintains intensive attention to detail thus resulting in a high reliability product. Generates, elicits, and maintains a productive work environment.

EXPERIENCE:
Electronics Engineer
Integral Solutions Int'l, Santa Clara, CA   2004 to Aug 2007

High volume printed circuit board layout of high performance Hard Disk Read/Write Head probe cards for high bandwidth Quasi-Static test instrument. Controlled impedance trace layout (to 1.2GHz) for signal analysis of +10 micro-volt level noise generated by R/W heads under magnetic field. Rigid dimensional criteria with numerous placement restrictions and exact polygon copper shapes. Connectivity varies between vendor Read/Write head preamplifiers requiring complex datasheets to determine characteristic impedances, signal descriptions, PECL levels etc.

Developed Hot/Cold option for bench top model Quasi Static tool; this facilitated testing of R/W heads under controlled temperatures from 5° to 120° Celsius. This cost effective design used a basic TE Cooler, custom modified OEM temperature controller, existing magnet power supply, and a small custom board for signal conversion.

Implemented SOP-39 Safety upgrades to capital equipment in-line Quasi Static tool. Designed Mains Interlock Box to EN-61010 compliance with multi-level cut off, door switches, EMO, and status logic. Product version passed the Safety Agency audit first time and was accepted by the specifying customer without incident. Design changes made were then implemented in all tool versions.

Responsible for sustaining designs of sub-systems and varied PCBAs. Was a major contributor to transfer of large in-line mechatronic assembly to offshore turn-key manufacturer. Provide comprehensive documentation, test procedures/fixtures, find hard to locate components, and make part substitutions etc. Active in supporting manufacturing test on production problem PCBA's. On call to repair field service returns not repairable by production.

Using OrCAD V9.1 for schematic capture and PCB layout; with PADS for all new PCB layouts over last 12 months. Maintain and upgrade large database of schematics and PCB files. Generate comprehensive BOMs, pick and place files, assembly drawings, part symbols and footprints. Many advanced OrCad skills: Back annotation, import/export part and net properties, Custom TitleBlocks with filespec, date/time stamps, NDA, and corporate information displayed automatically. Always have zero error Design Rules Checks.

Developed closed loop magnet control circuit for +/-1.85T high field version of in-line tester. I am listed as a co-inventor on submitted patent application.

This company has made significant increases in profitability during my employ; information of which may be obtained by referral.

Electrical Design Engineer
F.E.I. COMPANY (Acquired Surface Interface on 08-15-01), Sunnyvale, CA   1998 to 2003

Assigned Engineering Project Lead of Beta level Stylus-NanoProfilometer Hardware Development. SNP tool needed to be finished for customer acceptance testing in short time frame. Finished designs of electronic motion control, and electro-mechanical sub-systems; additionally cable assemblies, Mains power distribution, UPS power distribution, chassis parts, cameras, microscopes, and principle for CE Mark compliance. Shipped Beta unit on schedule, passed on-site acceptance testing and received prompt payment.

Principle designer of 3 angstrom resolution Capacitive Distance Measurement PCBA, I utilized complex OpAmp and signal generation circuits to achieve 30_{ppm} accuracy. Built pilot production run then released and shipped to customer base / F.G.I.

DAQ PCBA is not performing to 16 bit accuracy even with large sample size averaging. I designed higher performance replacement with 3X speed increase and 16 bit accuracy with small sample size. This allowed for increased through-put and enhanced CD measurement resolution on SNP.

PCI bus End Point / ISA bus Bridge PCBA retrofit to customer base will not be ready by promised ship date. Work over weekend to load firmware, debug circuits, upgrade provided test software, repair and test 5 each PCBA sets.   Shipped retrofit board sets to customer base as functional on Monday evening for 100% success and ahead of schedule.

Improved over 14 PCB's on existing layouts which were then ECO'ed. For over 40 cable assemblies, was the principle designer generating schematics, BOMs and related release information. Created numerous calibration and test fixtures for SNP analog electronics, also test hardware/software for proprietary bus P.C. boards and PCI End Point/ISA Bridge. Wrote many test procedures and trained Field Service and Test/Assemblers on circuits and systems. Performed large product documentation transfer to new company owner's ERP system meeting specific formats.

Mains Power Interlock Sub-system is hard to manufacture. Need SEMI S2-0302 compliant sub-system with PCBA that is easy to assemble. Design circuit and layout PCB that meets all compliance requirements for Mains power traces such as creepage, clearance, and ampacity. Meet or exceed all EN-61010 requirements for the sub-system such as safety ground, wire insulation, wire ampacity, and interrupting capacity. This was very successful and passed SEMI S2-0302 without incident and met all additional customer in-house requirements such as EMO interlock, and EMO accessory powering.

Implemented SEMI S2-0302, S2-0200 and 3rd party CE Mark safety certifications for SNP as acting division Safety Officer.

Design and build electrical wiring harness for MECA Sample Wheel / Translation Stage on Phoenix 2007 Mars Lander. Test reliability with extensive motion control script using OEM step motor controller.

Sustaining Engineer
LUXTRON CORP. (DBA: Lumasense Technology), Santa Clara, CA   1991 to 1998

Support broad range of process control instruments; re-design products for cost reduction and CE Marking compliance. Determine cause and solution to design flaws in existing products, and then implement solutions through an ISO-9001 approved IRN / ECO process.

EDUCATION: Computer Programming from DeAnza College: Pspice V9.2, VBasic, UNIX, OOP, C++, C, Scientific Pascal, and MASM with SJSU Programming, Math, and Physics transfer requirements completed. Associate in Arts from Cabrillo College